REMARKS

Claims 2 and 3 were previously cancelled. Claims 1 and 12 are amended. New claim 14 is added. No new subject matter is present. Reconsideration and allowance of claims 1 and 4-14 is requested in light of the following remarks.

Claim Rejections – 35 USC § 102

Claims 1, 4-6, and 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,188,976 to Kume et al. (hereafter, 'Kume'). The applicant disagrees.

Claims 1 and 12 are amended to recite, *inter alia*, the feature of "***prior to formation of the tunnel oxide layer and the gate oxide layer***, implanting impurity ions into the first and second active regions ***to adjust a threshold voltage of a MOS transistor***" (emphasis added). The above amendment to claims 1 and 12 consisted only of the deletion of a recited feature, thus, no new subject matter is added.

Kume (column 9, lines 53-63) teaches that a gate oxide film 16 is deposited after the p-type well region 12 and n-type well region 13 is formed. However, contrary to claims 1 and 12, Kume does not teach the recited feature of implanting impurity ions into the first and second active regions ***to adjust a threshold voltage of a MOS transistor*** prior to formation of the tunnel oxide layer and the gate oxide layer (emphasis added). Rather, as described above, Kume teaches that the impurity ions are implanted to form the well regions 12 and 13, not to adjust a threshold voltage.

Consequently, Kume fails to anticipate claims 1 and 12 because it does not show the identical invention in as complete detail as contained in the claims. MPEP 2131, *citing* Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236 (Fed. Cir. 1989).

Claims 4-6, 9-11, and 13 depend from claim 1. Thus, Kume does not anticipate claims 4-6, 9-11, and 13 because it fails to teach every feature inherent to the claims (MPEP 2131).

Claim Rejections – 35 USC § 103

Claims 1, 4-6 and 8-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Publication No. 2002/0008278 A1 attributed to Mori ('Mori') in view of U.S. Patent No. 5,292,681 to Lee et al. ("Lee"). The applicant disagrees.

Claims 1 and 12 recite, *inter alia*, the feature of "prior to formation of the tunnel oxide layer and the gate oxide layer, ***implanting impurity ions*** into the first and second active regions ***to adjust a threshold voltage of a MOS transistor***" (emphasis added).

The Examiner has agreed that Mori does not teach the feature recited above. Instead, it is alleged that Lee FIGs. 19-21 and 25-26 disclose this feature. Although the Examiner

does not give specifics as to which particular figure teaches the above feature , it is apparently alleged that Lee's FIG. 19 teaches the recited feature because it is FIG. 19 that illustrates the process step where the N-well 9 and the P-well 18 are formed (column 8, line 66 to column 9, line 3).

To the contrary, Lee states, in regard to FIG. 19, that "the wafer is subjected to a ***high temperature drive step*** which causes the boron atoms in original P-layer 121 and the phosphorous atoms in original N-type layer 123 to ***diffuse*** deeper into the substrate, creating a N-well 9 and a P-well 18" (column 8, line 67 – column 9, line 3; emphasis added).

It is apparent from the use of the terms "high temperature drive step" and "diffuse" when describing FIG. 19 that Lee is teaching the use of a ***diffusion process*** rather than an ***ion implantation process*** (emphasis added). "Diffusion" is the common name for a high-temperature doping process during which dopant atoms (not ions) are introduced into a semiconductor by diffusion of the dopant atoms. On the other hand, the feature of "implanting impurity ions" as recited in claims 1 and 12 refers to the process of accelerating dopant ions (not atoms) towards a solid surface so that the dopants penetrate the solid to a certain depth according to the ion energy. In other words, "diffusion" as taught by Lee FIG. 19 is a fundamentally different process than "implanting impurity ions" as taught by the applicant.

Furthermore, Lee states that the diffusion process creates a N-well 9 and a P-well 18 (column 9, line 3). Thus, Lee additionally does not teach the feature of implanting impurity ions ***to adjust a threshold voltage*** of a MOS transistor prior to forming the gate oxide layer and the tunnel oxide layer (emphasis added).

For the above reasons, the Mori/Lee combination fails to establish a *prima facie* case of obviousness for claims 1 and 12 because it fails to teach or suggest all the features of the claims (MPEP 2143.03).

Claims 4-11 and 13 depend from claim 1. Consequently, claims 4-11 and 13 are patentable over the Mori/Lee combination because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03, citing In re Fine, 837 F.2d 1071 (Fed. Cir. 1988).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of U.S. Patent No. 5,976,934 to Hayakawa ("Hayakawa"). The applicant disagrees.

Claim 7 depends from claim 1. Consequently, claim 7 is patentable over the Mori/Lee/Hayakawa combination because any claim that depends from a nonobvious

independent claim is also nonobvious. MPEP 2143.03, citing In re Fine, 837 F.2d 1071 (Fed. Cir. 1988).

New Claim 14

New claim 14 is added that depends from claim 1. The subject matter featured in claim 14 is fully supported by the original application at, e.g., page 6, lines 28-31.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 1 and 4-14 of the application as amended is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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